Electrical Instability of RF Sputter Amorphous In-Ga-Zn-O Thin-Film Transistors

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(Invited Paper)

***Abstract*—Bias-temperature-stress (BTS) induced electrical instability of the RF sputter amorphous In-Ga-Zn-O (a-IGZO) thin-film transistors (TFTs) was investigated. Both positive and negative BTS were applied and found to primarily cause a positive and negative voltage shift in transfer ($I_{\rm DS} - V_{\rm GS}$) characteristics, respectively. The time evolution of bulk-state density ($N_{\rm BS}$) and characteristic temperature of the conduction-band-tail-states (T_G) are extracted. Since both values showed only minor changes after BTS, the results imply that observed shift in TFT $I_{\rm DS} - V_{\rm GS}$ curves were primarily due to channel charge injection/trapping rather than defect states creation. We also demonstrated the validity of using stretch-exponential equation to model both positive and negative BTS induced threshold voltage shift ($\Delta V_{\rm th}$) of the a-IGZO TFTs. Stress voltage and temperature dependence of $\Delta V_{\rm th}$ evolution are described.**

***Index Terms*—a-IGZO, amorphous semiconductors, bias temperature stress (BTS), semiconductor device reliability, transparent thin-film transistors (TFTs).**

I. Introduction

ALTHOUGH the hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) has long been the workhorse for active-matrix liquid crystal display (AM-LCD), its low mobility restricts the TFT high frequency response and current driving capability. This disadvantage becomes a limiting factor for display performance, especially when the current trends of active-matrix flat panel display (AM-FPD) development are toward high frame rate (120–240 Hz) [1] and "all solid-state" device, such as active-matrix organic light-emitting display (AM-OLED) [2], [3]. On the other hand, poly-crystalline silicon (poly-Si) TFT is considered as a high mobility alternative device. However, such technology usually required additional crystallization steps (e.g., excimer laser annealing [4], metal seeding [5] or solid phase crystallization [6]) which raise more concerns when manufacturing over large substrate area is considered [3]. During the past few years, there have been great interests in using amorphous In-Ga-Zn-O (a-IGZO) thin-film transistor (TFT) in AM-FPDs [7]–[11]. Because the electrons are drifting through ionic metal s-orbital, which permit a band-like conduction even in amorphous phase, a-IGZO TFTs have a higher field-effect mobility ($\mu_{\rm eff}$) than traditional covalent bond semiconductors (e.g., a-Si:H) [7]. These properties make a-IGZO TFTs one of the ideal choices for future large area (e.g., 82-in) ultra-definition (up to $4k \times 4k$ pixels, [12], [13]) display backplane technology.

To ensure a robust product based on a-IGZO TFTs, it is essential to evaluate their electrical stability. The long-term constant current- temperature stress (CTS) study has shown that the a-IGZO TFT has a stable electrical properties with a threshold voltage shift ($\Delta V_{\rm th}$) much smaller (0.2 V) than the $\Delta V_{\rm th}$ for a-Si:H TFT (> 1.8 V) under the same AM-OLED testing condition (3 μA, 60 °C, 20 hours) [14]. The proper passivation layer for the back channel was also found to play an important role in improving the TFT CTS reliability [8]. Recent studies further extended investigation of a-IGZO stability into the bias-temperature stress (BTS) measurements. A positive shift in TFT $V_{\rm th}$ was observed under a positive (gate bias) BTS while the $V_{\rm th}$ shifted to negative values for negative BTS [15]. Furthermore, a simple power law relation is able to fit the stress time trend of measured $\Delta V_{\rm th}$ [16]. A great reduction ($\sim 75\%$) in BTS induced degradation was found when additional post thermal annealing step during fabrication is performed. Although the nature of this reduction is not clear, the defect states located in bulk active layer or near the interface are suspected to be of its origin [15].

Despite all the progress in a-IGZO TFTs so far, our knowledge of the physical origin of its electrical stability is very limited, and should be addressed more in-depth. In this paper, we report the detailed study of the initial electrical properties and BTS induced electrical instability of RF sputter a-IGZO TFTs. Proper simulation model is also proposed to describe experimental data.

II. Experimental

A. TFT Structure

The cross-sectional view of the a-IGZO TFT used in this study is shown in Fig. 1(a). The detail processing steps were discussed elsewhere [11]. The TFT has an inverted-staggered bottom-gate structure. The Ti/Au/Ti stacking layers are used for gate and source/drain (S/D) electrodes. The SiO_2 gate insulator and a-IGZO active layer is about 200 and 30 nm thick, respectively. Both layers are deposited by RF magnetron sputtering. After the island formation and S/D electrodes definition, an additional sputter SiO_2 capping layer is added which serves as a

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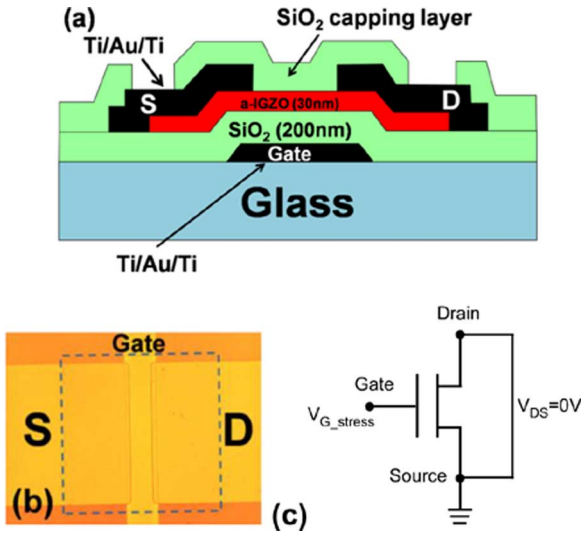

Fig. 1. (a) Cross-setional and (b) top view of the RF sputter a-IGZO TFT device used in this study. Dash square indicates the region of a-IGZO active layer. (c) The schematic of the circuit setup used for steady state BTS experiments.

protection layer for the TFT back channel. Finally, a thermal annealing strep (200 °C, 1 hour in air) is applied. The die photo of the final RF sputter a-IGZO TFT is shown in Fig. 1(b).

B. Electrical Measurement

To understand the initial electrical performance, electrical properties of a-IGZO TFT were analyzed in detail by using a semiconductor parametric analyzer (Agilent 4156C) and a light-tight probe station. Later, a series of BTS experiments were conducted for steady-state conditions using the same setup. During the BTS, a predetermined stress voltage (V_{G_stress}) is applied to the gate electrode and to ensure a uniform electrical field distribution along the SiO_2/a-IGZO interface, the drain terminal of the TFT is short to its source terminal ($V_{\mathrm{DS}} = 0$ V, Fig. 1(c)). Measurements were also performed under different stress temperatures (T_{STR}) ranging from 50 °C–80 °C. For even lower temperature, the ΔV_{th} is too small (few 10 mV) to make a reliable analysis within the BTS time range (10 Ks) chosen in this study. It should be noticed that all the BTS induced electrical instability can be fully recover after thermal annealing step (2 hours, 200 °C, as illustrated in Fig. 11). Each series of BTS experiment is performed on the same TFT and to ensure consistent initial TFT properties, the thermal annealing is applied before each new BTS experiment is conducted.

III. Electrical Performance of a-IGZO TFT

A. a-IGZO TFT Electrical Properties

The output characteristics of a-IGZO TFT under various gate voltages (V_{GS}) ranging from 0 to 20 V are shown in Fig. 2(a). During each measurement, the drain voltage (V_{DS}) was varied from 0 to 20 V. A very clear distinction between linear and saturation region is obtained. This suggests that less than 20 V of drain voltage (V_{DS}) is adequate for operating a-IGZO TFT active-matrix arrays. The other important aspect for evaluation is TFT source–drain property. TFT with a non-ohmic source/drain contact, improper active layer thickness (too thick) or high bulk density of states (DOS) can have a nonlinear drain current $(I_{\mathrm{DS}})/V_{\mathrm{DS}}$ behavior, also called "current crowding", at low V_{DS} [17], [18]. Fig. 2(b) shows the output characteristics near the origin ($V_{\mathrm{DS}} = 0 \sim 2.5$ V) and there is no current crowding observed in a-IGZO TFT when Ti/Au/Ti electrodes are used. The absence of current crowding can be better appreciated by plotting the derivative of the output curves $(\delta I_{\mathrm{DS}}/\delta V_{\mathrm{DS}})$ which is also shown in Fig. 2(b). These properties are highly desirable for a-IGZO TFT to be used in active-matrix arrays.

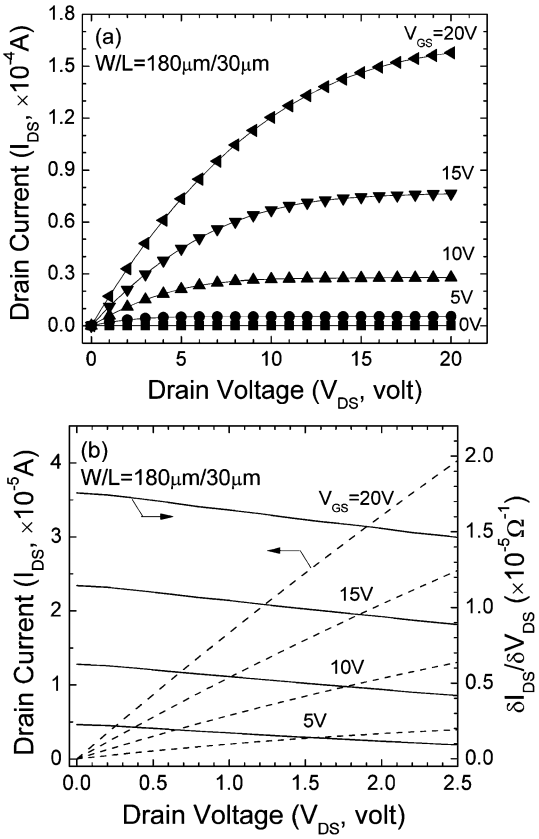

Fig. 2. (a) Output characteristics of RF sputter a-IGZO TFT. (b) A zoom-in plot of the output characteristics (dash curves) near origin ($V_{\mathrm{DS}} = 0 \sim 2.5$ V); the derivative of I_{DS} vs. V_{DS} ($\delta I_{\mathrm{DS}}/\delta V_{\mathrm{DS}}$, solid curves) are also shown.

Fig. 3(a) illustrates the transfer characteristics of a-IGZO TFT. We extracted the threshold voltage (V_{th}) and field effect mobility (μ_{eff}) based on the standard MOSFET equation in both linear region ($V_{\mathrm{DS}} = 0.1$ V):

$$I_{\mathrm{DS}} = \mu_{\mathrm{eff}} C_{\mathrm{ox}} \left(\frac{W}{WL}\right) (V_{\mathrm{GS}} - V_{\mathrm{th}}) V_{\mathrm{DS}} \tag{1}$$

and saturation region ($V_{\mathrm{DS}} = 20$ V):

$$(I_{\mathrm{DS}})^{1/2} = \left[\mu_{\mathrm{eff}} C_{ox} \left(\frac{W}{2L}\right)\right]^{1/2} (V_{\mathrm{GS}} - V_{\mathrm{th}}) \tag{2}$$

where C_{ox} is the gate insulator capacitance per unit area, W and L are TFT channel width and length, respectively. The straight lines in Fig. 3(a) represent the best linear fit of (1) and (2) between 90% to 10% of the maximum I_{DS} (or $(I_{\mathrm{DS}})^{1/2}$) at $V_{\mathrm{GS}} = 20$ V. The subthreshold swing (S) was also extracted

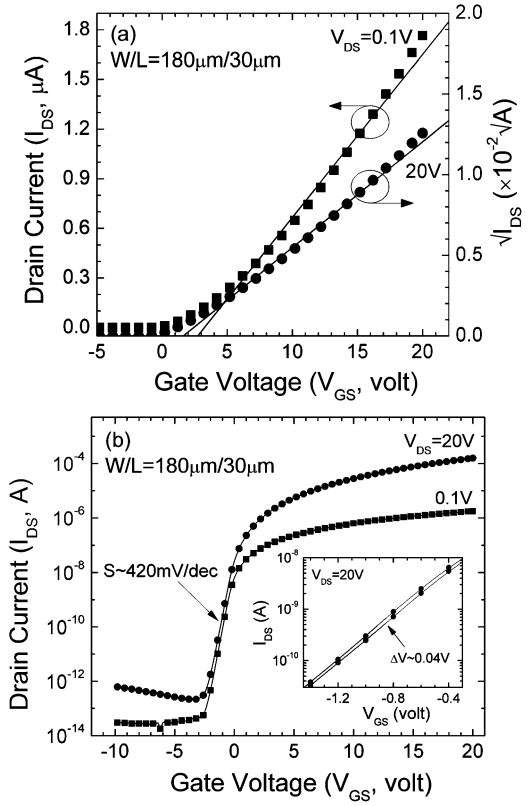

Fig. 3. Transfer curves of a-IGZO TFT in (a) linear and (b) semi-log scales. (Inset, b) The TFT hysteresis measured at $V_{\rm DS} = 20$ V; ΔV is the shift in sub-threshold properties. Symbol (•) and (■) represent the saturation ($V_{\rm DS} = 20$ V) and linear ($V_{\rm DS} = 0.1$ V) region properties, respectively.

at the maximum slope point ($V_{\rm GS} = -1.4$ V) from the sub-threshold region data [Fig. 3(b)], using the following equation:

$$S = \left[\frac{\delta \log\left(I_{\rm DS}\right)}{\delta V_{\rm GS}}\right]^{-1}. \tag{3}$$

The S for the RF sputter a-IGZO TFT is around 420 mV/decade. Such sharp switching is compatible or even superior than some a-Si:H TFTs and ensured a fast transistor response with reduced voltage of gate driving signal. In case of the a-Si:H TFT, the subthreshold swing can be associated with the density of deep bulk states ($N_{\rm BS}$) and interface states (N_{SS}) at the interface between gate insulator and semiconductor layers by the following formula [19]:

$$S = \frac{kT}{q\log(e)}\left[1 + \frac{qd_{\rm ins}}{\varepsilon_{\rm ins}}\left(\sqrt{\varepsilon_{\rm semi}N_{\rm BS}} + qN_{SS}\right)\right] \tag{4}$$

where k, T, and q are the usual physical parameters; $\varepsilon_{\rm ins}$ and $\varepsilon_{\rm semi}$ are permittivity in insulator and semiconductor, respectively; and $d_{\rm ins}$ is the effective thickness of the insulator. If we assume the similar situation also occur in a-IGZO TFT, the bulk states of the a-IGZO active layer can be approximately estimated by considering a sole contribution from bulk states in (4) (set $N_{SS} = 0$). With the S of 420 mV/decade and the dielectric constant for a-IGZO of 10, we calculated the $N_{\rm BS}$ to be around 7.7×10^{16} eV^{-1}cm^{-3}. This value is consistent with the density extracted by SPICE modeling [20] and from a-IGZO TFT made by pulse-laser deposition (PLD) [21].

TABLE I
ELECTRICAL PROPERTIES OF RF SPUTTER a-IGZO TFT

Parameter	Unit	Value (region)	
$\mu_{\rm eff}$*	cm^2/Vs	Linear	9.51
		Saturation	8.3
$V_{\rm th}$*	V	Linear	3.23
		Saturation	1.63
S	mV/decade	420	
$I_{\rm DS\text{-}OFF}$	A	$<10^{-12}$	
On/off ratio**		$\sim10^8$	

* Extracted by 90%-10% method.
** "On/off ratio" is the drain current ratio between on and off states.

Table I summarizes all key TFT properties. Our RF sputter a-IGZO TFT have average $\mu_{\rm eff}$ of 8–9 cm^2/V·s, which is about ten times higher than typical a-Si:H TFT value (~ 0.8 cm^2/V·s). We also measured the TFT off-state drain current ($I_{DS_{\rm off}}$) down to $V_{\rm GS} = -10$ V. Although the $I_{DS_{\rm off}}$ is drain voltage dependent, the value is below 10^{-12} A. Moreover, TFT on/off ratio is maintained at 10^8 for both linear and saturation region. This indicates the film resistivity of a-IGZO is well under controlled during deposition [22].

B. Field-Effect Mobility of a-IGZO TFT

The $\mu_{\rm eff}$ extracted by (1) or (2) can be considered as average value. Further analysis of the linear region transfer data [Fig. 3(a)] reveals a nonlinear $I_{\rm DS}/V_{\rm GS}$ behavior observed at the higher $V_{\rm GS}$: the $I_{\rm DS}$ seems to be higher than expected value for a given $V_{\rm GS}$. In other words, the apparent field-effect mobility is dependent on $V_{\rm GS}$. This can be better illustrated by defining the incremental field-effect mobility ($\mu_{\rm inc}$) with the following relation:

$$\mu_{\rm inc} = \left(\frac{\delta I_{\rm DS}}{\delta V_{\rm GS}}\right)\left[\frac{L}{(WC_{\rm ox}V_{\rm DS})}\right] \tag{5}$$

and plots it as a function of $V_{\rm GS}$. As shown in Fig. 4, $\mu_{\rm inc}$ of a-IGZO TFT is proportional to the $V_{\rm GS}$ and reaches a maximum value 12.6 cm^2/V·s within our measurement range, but $\mu_{\rm inc}$ does not saturate. Such behavior has also been seen in other oxide semiconductor TFTs [23], [24]. It is believed that portion of the induced channel charges are trapped in band tail states (or deep states) and cannot contribute to the $I_{\rm DS}$. As $V_{\rm GS}$ increased, more free carriers are able to contribute to the $I_{\rm DS}$ and this makes $\mu_{\rm inc}$ increase toward the intrinsic band mobility (intrinsic band mobility of 15 cm^2/V·s was used in the numerical simulation of RF sputter a-IGZO TFT with thermal SiO_2 as gate insulator [25]). Therefore, to better model the a-IGZO TFT I/V properties, the gate voltage dependent field-effect mobility ($\mu_{\rm eff}(V_{\rm GS})$) is introduced into the standard MOSFET equation [see (1)]

$$I_{\rm DS} = \mu_{\rm eff}\left(V_{\rm GS}\right)C_{ox}\left(\frac{W}{L}\right)\left(V_{\rm GS} - V_{\rm th}\right)V_{\rm DS} \tag{6}$$

and $\mu_{\rm eff}(V_{\rm GS})$ can be described as

$$\mu_{\rm eff}\left(V_{\rm GS}\right) = \mu_0\left[\frac{(V_{\rm GS} - V_{\rm th})}{V_C}\right]^{\alpha} \tag{7}$$

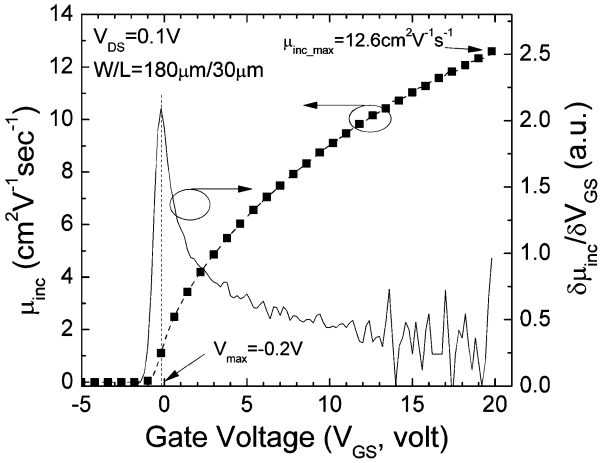

Fig. 4. Symbol (■): The incremental field-effect mobility ($\mu_{\rm inc}$) of a-IGZO TFT extracted by using (5). The differentiation of $\mu_{\rm inc}$ ($\delta\mu_{\rm inc}/\delta V_{\rm GS}$, solid line) is also shown. $V_{\rm max}$ represents the $V_{\rm GS}$ with maximum $\delta\mu_{\rm inc}/\delta V_{\rm GS}$.

where μ_0 is the intrinsic band mobility, V_C is the material dependent critical voltage and α is the power coefficient which describes the dependence of $\mu_{\rm eff}(V_{\rm GS})$ on effective gate voltage $(V_{\rm GS} - V_{\rm th})$. As a comparison, in ideal case, $\alpha = 0$ and $\mu_{\rm eff}(V_{\rm GS}) = \mu_{\rm eff} = \mu_0$. For the ease of parameter extraction, (7) is further simplified as

$$\mu_{\rm eff}\left(V_{\rm GS}\right) = K\left(V_{\rm GS} - V_{\rm th}\right)^{\alpha} \tag{8}$$

where K is the material dependent fitting parameter. It should be noticed that the K has the unit of $\mathrm{cm}^2/V^{\alpha+1}\mathrm{s}$. By substituting (8) into (6), new $I_{\rm DS}$ equation can be written as

$$I_{\rm DS} = KC_{ox}\left(\frac{W}{L}\right)\left(V_{\rm GS} - V_{\rm th}\right)^{\gamma} V_{\rm DS} \tag{9}$$

$$\text{where } \gamma \equiv \alpha + 1. \tag{10}$$

From (8) and (10), we can also derive:

$$\mu_{\rm eff}\left(V_{\rm GS}\right) = K\left(V_{\rm GS} - V_{\rm th}\right)^{\gamma-1} \tag{11}$$

and from (5) and (9), incremental field-effect mobility can be described as

$$\mu_{\rm inc} = K\gamma\left(V_{\rm GS} - V_{\rm th}\right)^{\gamma-1}. \tag{12}$$

Special care should be made to properly extract the $V_{\rm th}$, γ and K. Directly performed a nonlinear fitting of the entire transfer data to (9) is not an ideal approach because this can introduce unwanted subthreshold region data into the fitting algorithm which causes error. In this study, we propose two different methodologies which are suitable for device parameter extraction. The first method (method #1) is adapted from what was developed for a-Si:H TFT [26]. The determination of threshold voltage is based on (9). By varying $V_{\rm th}$, we find the least-square linear fit to the logarithm of drain current ratio

$$\log\left(\frac{I_{\rm DS}}{I_0}\right) = \gamma\log\left(\frac{V_{\rm GS} - V_{\rm th}}{V_0 - V_{\rm th}}\right) \tag{13}$$

where the reference drain current, $I_0 = I_{\rm DS}(V_{\rm GS} = V_0)$, is chosen to be much larger than the subthreshold current. In this study, $V_0 = 5$ V with $I_0 = 2.29 \times 10^{-7}$ A were chosen.

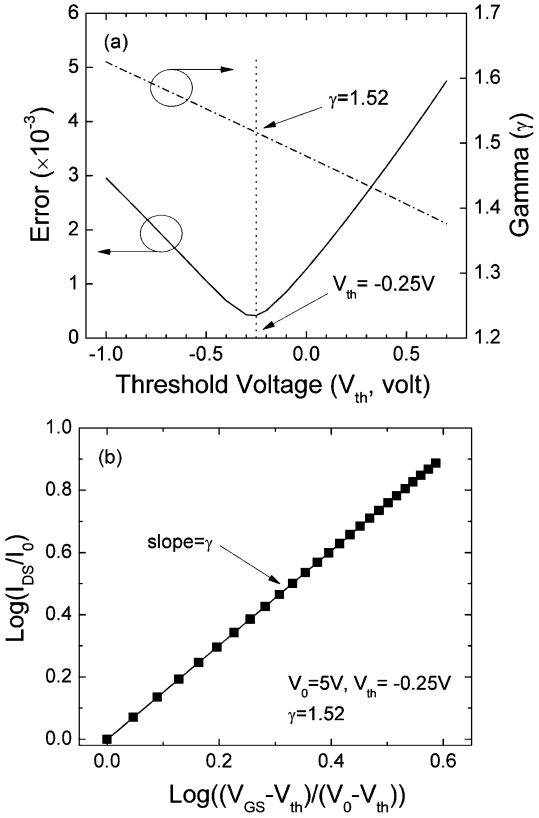

Fig. 5. (a) Variation in γ of the experimental I-V data in above threshold region as a function of $V_{\rm th}$. A reference gate voltage V_0 of 5 V is used for parameter extraction. Also shown is the rms error of the least-square fit to the log of drain current ratio ($\mathrm{Log}(I_{\rm DS}/I_0)$). (b) Example of the actual linear fitting plot to (13) at $V_{\rm th}$ with minimum error (-0.25 V).

Fig. 5(a) shows the RMS error and corresponding γ of the linear fit to (13) as a function of $V_{\rm th}$. The $V_{\rm th}$ and γ are determined simultaneously by the best linear fit with minimum error. As indicated in Fig. 5(b), $V_{\rm th}$ and γ are -0.25 V and 1.52, respectively. $K(= 1.76)$ is finally extracted by performing a best nonlinear fit of above threshold transfer data to (9). Although the first method (method #1) can accurately extract $V_{\rm th}$ and γ simultaneously, the procedure is rather complicated and not straight forward. Our second approaches (method #2) extract $V_{\rm th}$, γ and K separately in a two-step process. A similar method has also been used to extract the threshold voltage of the a-Si:H TFT [27]. The $V_{\rm th}$ is first defined as the $V_{\rm GS}$ value at which maximum $d\mu_{\rm inc}/dV_{\rm GS}$ occurs ($V_{\rm max} = V_{\rm th} = -0.2$ V, as illustrated in Fig. 4). The "change" of $\mu_{\rm inc}$ vs $V_{\rm GS}$ has two opposite behaviors between sub- and above threshold regions: in subthreshold region, $\mu_{\rm inc}$ increases exponentially with $V_{\rm GS}$ and the $d\mu_{\rm inc}/dV_{\rm GS}$ is increasing with $V_{\rm GS}$. However, in above threshold region, $d\mu_{\rm inc}/dV_{\rm GS}$ is decreasing with $V_{\rm GS}$, and $\mu_{\rm inc}$ will eventually saturate at certain value (e.g., intrinsic band mobility, μ_0). Consequently, the maximum $d\mu_{\rm inc}/dV_{\rm GS}$ point represents the transition between these two regions, where $V_{\rm th}$ is located. The authors believe such phenomenon is fundamentally due to the difference in a-IGZO deep gap and band tail density-of-states (DOS) properties. The $\gamma - 1$ (or α) and K are then extracted from the linear fit of the log-log plot of (12)

$$\log\left(\mu_{\rm inc}\right) = \log\left(K\gamma\right) + (\gamma - 1)\log\left(V_{\rm GS} - V_{\rm th}\right) \tag{14}$$

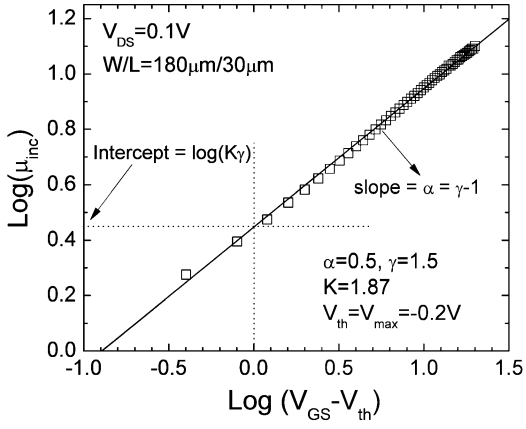

Fig. 6. The log–log plot of the incremental field-effect mobility ($\mu_{\rm inc}$) as a function of the effective gate voltage ($V_{\rm GS} - V_{\rm th}$). The $V_{\rm th}$ is extracted from $V_{\rm max}$ in Fig. 4. Solid line is the linear fit to the experimental data (symbol: □).

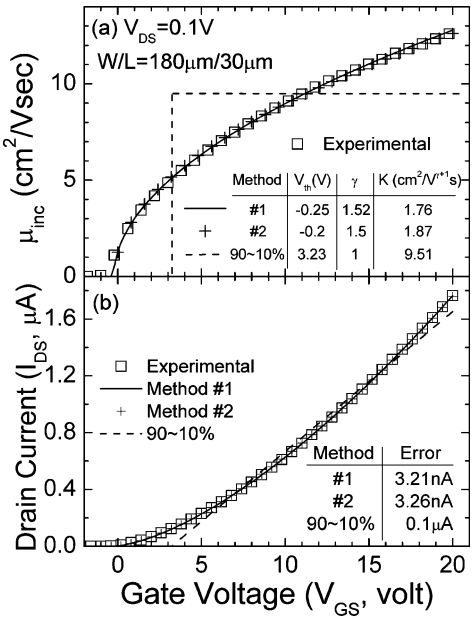

Fig. 7. The calculation of (a) $\mu_{\rm inc}$ and (b) $I_{\rm DS}$ based on different models/extraction methods used in this study. Method #1 (solid line) is conducted in Fig. 5. Method #2 (+) is illustrated in Fig. 6. The 90%$\sim$ 10% method (dash line) is conducted based on the standard MOSFET equation ((1)). Symbol (□): experimental data.

as shown in Fig. 6. In summary, the $V_{\rm th}$, γ and K extracted by method #2 are $-$ 0.2 V, 1.5 and 1.87, respectively.

Fig. 7. shows the results obtained from various models/methodologies discussed in this study. The table in Fig. 7(a) summarized the extracted parameters by using different methods. The $\mu_{\rm inc}$ and $I_{\rm DS}$ are calculated by substituting corresponding parameters into (12) and (9), respectively. Results obtained from method #1 and #2 are consistent with each other and they are fairly closed to the experimental data. RMS errors for $I_{\rm DS}$ calculated by different methods are also provided in Fig. 7(b) and method #1 has the lowest error. It is clear that the (8) is suitable for describing gate voltage dependent field-effect mobility, $\mu_{\rm eff}(V_{\rm GS})$, which is essential to accurately model the a-IGZO TFT I/V properties. The extracted γ of our RF sputter a-IGZO TFT is slightly higher than the value of a-IGZO TFT made by pulse-laser deposition (PLD) ($\gamma = 1.37$) [28] and of coplanar homo-junction a-IGZO TFT with chemical vapor deposition (CVD) SiO_2 gate insulator ($\gamma = 1.13$) [29]. This suggests that γ is affected not only by the deposition method of IGZO but also by the gate insulator, fabrication processes, and device structures. In fact, the significance of γ is often given by

$$\gamma = 2\left(\frac{T_G}{T}\right) - 1 \tag{15}$$

where T is the temperature and T_G is the characteristic temperature of the amorphous semiconductor DOS distribution around the position of the Fermi level.[30] The equation is valid for $T < T_G$. For a-Si:H, T_G commonly represents the characteristic temperature of the conduction-band-tail-states and a high density of such states causes the nonideal condition of $\gamma > 1$. Suppose the same mechanism also held for a-IGZO TFT, we extracted the T_G from our a-IGZO TFT to be ~ 371 K (or $kT_G \sim 32$ meV). It should be noticed that the actual T_G for a-IGZO conduction-band-tail-states might have an even lower value, due to the limitation of room temperature measurement. Nonetheless, the authors suppose that the extracted T_G is still proportional to the density of conduction-band-tail-states, i.e., a higher γ can correspond to an increase in T_G and vice versa.

IV. a-IGZO TFT Electrical Instability

A. Steady-State BTS Experiments

A series of BTS experiments were conducted and the experimental details have been discussed in Section II-B if not specify individually. We monitored the evolution of device degradation by interrupting the BTS at predetermined time steps and measuring the TFT transfer properties. During BTS measurement, the $V_{\rm th}$ of TFT is continuously changing. Since the $V_{\rm GS}$ range for the transfer property measurement is fixed, the maximum achievable drain current ($I_{DS\text{-MAX}}$) is varying during different BTS time steps. This causes the traditional $90\% \sim 10\%$ method, which relies on $I_{DS\text{-MAX}}$ to determine the analyzing data range, to be unsuitable due to the unequal data range among data collected at different times. In order to ensure a consistent comparison of extracted parameters between different BTS time steps, a fixed data range should be defined. In this study, all the TFT $V_{\rm th}$ and $\mu_{\rm eff}$ were extracted from the linear fit of the saturation region transfer curves between $(I_{\rm DS})^{1/2} = 0.01 \sim 0.001$ A$^{1/2}$ to the standard saturation region MOSFET equation [see (2)], as illustrated in Fig. 8. Here, $V_{\rm DS} = 20$ V rather than $V_{\rm DS} = V_{\rm GS}$ was chosen because the first condition allows the TFT sub-threshold region properties to be precisely measured. The $\Delta V_{\rm th}$ is calculated as the difference between threshold voltages extracted at each stressing time step and the initial values of each BTS experiment ($V_{th\_\rm initial}$). Sub-threshold swing (S) is extracted from transfer characteristic in sub-threshold region, using (3). In addition, to better characterize the change in sub-threshold region, the parameter ΔV_T is defined as the transfer properties shift at $I_{\rm DS} = 10^{-9}$ A.

Fig. 8(a) shows the typical results we observed during the positive BTS experiments. The linear plots show a positive shift in TFT I-V properties and are consistent with the trend of $\Delta V_{\rm th}$ extracted. The negative BTS experiment is also performed at 80°C with $V_{G\_\rm stress} = -20$ V (Fig. 8(b)). A uniform negative shift is observed in both on and sub-threshold regions. Key

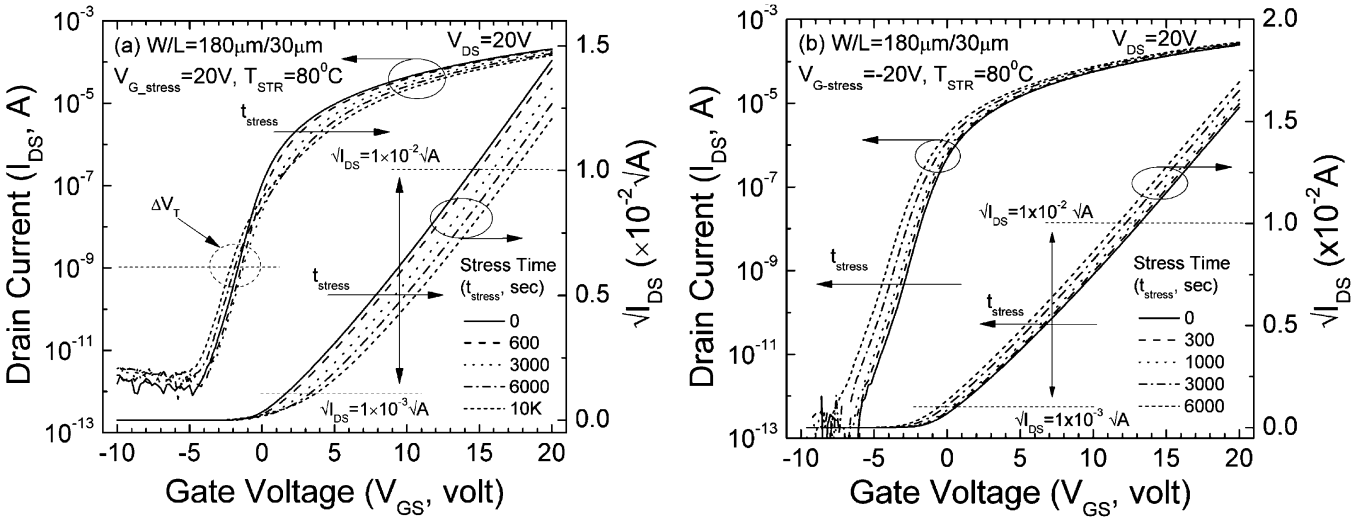

Fig. 8. The evolution of RF sputter a-IGZO TFT transfer characteristics for (a) positive BTS ($V_{G\_\mathrm{stress}} = 20$ V) and (b) negative BTS ($V_{G\_\mathrm{stress}} = -20$ V). For both experiments, the stress temperature, T_{STR}, is 80°C.

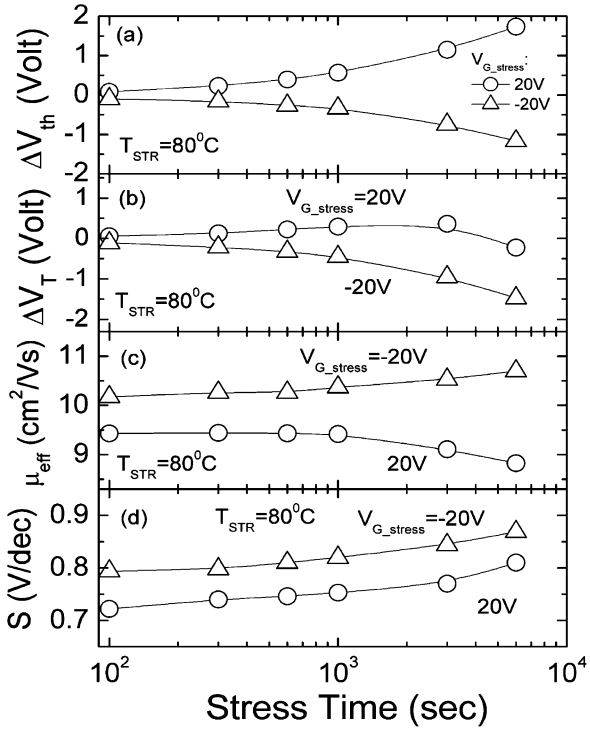

Fig. 9. (a) ΔV_{th}, (b) ΔV_T, (c) μ_{eff} and (d) S as a function of stress time (t_{stress}) for both positive ($V_{G\_\mathrm{stress}} = 20$ V) and negative (-20 V) BTS. Symbols represent the experimental data and lines are for aid of eye.

parameters such as ΔV_{th}, ΔV_T, μ_{eff} and S are extracted and plotted as a function of stress time (t_{stress}) in Fig. 9. The result indicates that during the circuit operation, both positive and negative clock cycles can cause change in a-IGZO TFT electrical properties. Circuit designer should optimized the circuit driving scheme to ensure the product lifetime.

The BTS induced ΔV_{th} is the primary a-IGZO TFT instability. It should be noticed that a slight change in μ_{eff} and S is also observed (Fig. 9(c)&(d)). Many previous studies in amorphous semiconductor TFTs (e.g., a-Si:H TFT) have concluded that two main mechanisms can explain the electrical instability.[31]–[34] One is the carrier trapping in the gate insulator [31], [32] and the other is point defect creation which will increase the density of deep-gap (bulk) states at or near the semiconductor/gate insulator interface [33], [34]. In a-Si:H TFT, deep-gap states are originated from Si-Si weak and Si-dangling bonds. Biasing the TFT can cause the amorphous Si network to be unstable and the network can rearrange to break the Si-Si bonds.[35] However, in a-IGZO, instead of the sp^3 orbitals, carriers are conducting through metal ion's ns-orbitals with sufficient inter ions overlap.[7] Such mechanism permits a-IGZO to have a high immunity to dangling bond creation and maintains a low density of deep-gap states.[36] Fig. 10 illustrates the time evolution of bulk state density (N_{BS}) and characteristic temperature of the conduction-band-tail-states (T_G) extracted by using (4) and (15), respectively. The increases of N_{BS} for both BTS polarities are less than 30% by the end of BTS experiments. The variation of kT_G is very small and is fairly closed to ~ 34 meV. This indicates the conduction band-tail states weren't affected by the BTS. As a comparison, by the end of the experiments, ΔV_{th} is about 1.5–2 V for both BTS polarity. This corresponds to a relative change of $> 100\%$. Therefore, our experimental results support the previously proposed theory and ΔV_{th} can be attributed mainly to charge trapping with some minor contribution from defects creation.

The analysis of ΔV_T (Fig. 9(b)) highlights the difference between positive and negative BTS under longer stress time. Despite the positive shift in on-region, the sub-threshold properties (ΔV_T) for positive BTS are actually starting to shift negatively for $t_{\mathrm{stress}} > 3000$ s, which can also be seen in the semi-log plot in Fig. 8(a). This was accompanied by an increase (about two times) in the TFT off-current ($I_{DS_{\mathrm{off}}}$). On the other hand, negative BTS shows a consistent negative shift in both regions. The increase of $I_{DS_{\mathrm{off}}}$ can be much larger under a severe positive BTS condition with $V_{G\_\mathrm{stress}} = 27$ V, 40 Ks and T_{STR} of 80 °C as depicted in Fig. 11. The increased $I_{DS_{\mathrm{off}}}$ can be associated with the decrease in a-IGZO film resistivity. It is a reversible process even under the severe BTS and the TFT can

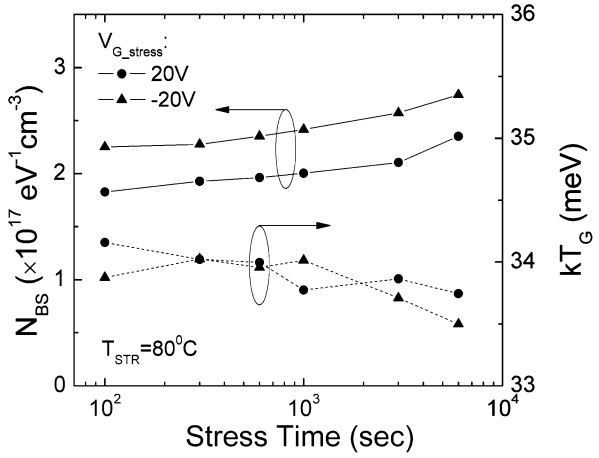

Fig. 10. Density of bulk-states ($N_{\rm BS}$) and characteristic temperature of conduction-band-tail-states (T_G) as a function of stress time ($t_{\rm stress}$) for both positive ($V_{G\_\rm stress} = 20$ V) and negative (-20 V) BTS.

TABLE II
FITTING PARAMETERS FOR STRETCHED-EXPONENTIAL MODEL

Model Parameters	Value	
	Positive BTS	Negative BTS
α	1.41	1.30
β	0.75	0.65
τ_0 (sec)	1.24×10^{-5}	2.2×10^{-25}
E_τ (eV)	0.78	2.16

recover to its initial state after the thermal annealing step discussed in Section II-B. Since the increase in either bulk-states or conduction band-tail states should cause the positive shift in TFT I/V properties [37], such negative ΔV_T shift observed for prolong positive BTS should be associated with other secondary effect, e.g., certain defect creation mechanism that only exists in metal oxide semiconductors. Many previous works of a-IGZO TFT have shown that the oxygen vacancy in a-IGZO can cause a decrease in film resistivity [22], [38] and a negative shift in TFT sub-threshold properties [39]. These reported phenomena are very similar to the a-IGZO I/V properties we observed after prolong positive BTS. Despite that the exact physical origin is still unclear, the authors suggest the meta-stable oxygen vacancies could be induced near the semiconductor/gate insulator interface by prolong positive BTS in this case. The induced oxygen vacancies then cause an increase in a-IGZO TFT $I_{DS_{\rm off}}$ and the negative shifts in TFT sub-threshold *I–V* properties (ΔV_T).

V. STRETCHED-EXPONENTIAL MODEL

To better understand the physics behind the BTS induced $\Delta V_{\rm th}$ in RF sputter a-IGZO TFT. We performed a detail numerical analysis based on the stretched-exponential model. The model, which was originally developed for AM-FPD based on charge injection/ trapping concept [32], [40], describe the TFT $\Delta V_{\rm th}$ by the following equation:

$$|\Delta V_{\rm th}| = |\Delta V_0|^{\alpha}\left\{1-\exp\left[-\left(\frac{t_{\rm stress}}{\tau}\right)^{\beta}\right]\right\} \quad (16)$$

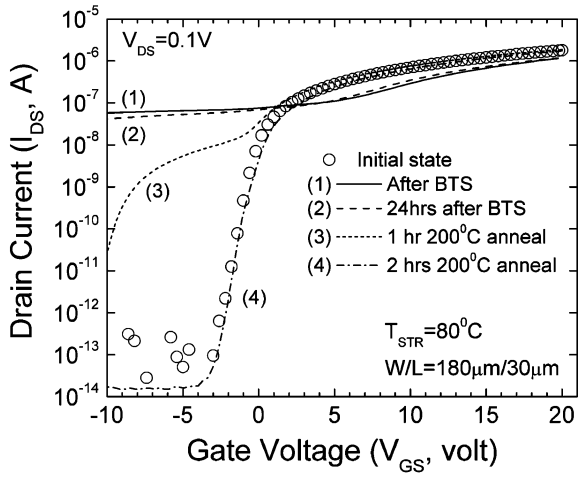

Fig. 11. Recovery of the a-IGZO TFT electrical instability after thermal annealing. (1) TFT transfer properties after severe BTS condition ($V_{G\_\rm stress} = 27$ V, $T_{STR} = 80$ °C, 40 Ks); (2) 24 hr of storage under room temperature after BTS; (3) after 1 hour and (4) 2 hours of thermal annealing (200 °C) in air.

$$\Delta V_0 = V_{G\_\rm stress} - V_{th\_\rm initial} \quad (17)$$

$$\tau = \tau_0 \exp\left(\frac{E_\tau}{kT_{STR}}\right). \quad (18)$$

In the above equations, ΔV_0 is the effective voltage drop across the gate insulator (or also called effective stress voltage); $V_{th\_\rm initial}$ is the initial threshold voltage; α is the exponent for ΔV_0 dependence and β is the stretched exponential exponent. The τ in (16) represents the characteristic trapping time of carriers and E_τ is the average effective energy barrier that carriers in conducting channel needed to overcome before they can enter the insulator or near interface region, with τ_0 being the thermal pre-factor for emission over barrier. For a very short stress time ($t_{\rm stress} \ll \tau$) (16) can be further shortening as

$$|\Delta V_{\rm th}| \cong |\Delta V_0|^{\alpha}\tau^{-\beta}t_{\rm stress}^{\beta}. \quad (19)$$

Equation (19) relates $\Delta V_{\rm th}$ to a straightforward power law dependence (β) of $t_{\rm stress}$ and has been applied to model BTS data. [11] On the other hand, for infinite stress time ($t_{\rm stress} \to \infty$), (16) will give a saturated behavior with $\Delta V_{\rm th} \to (\Delta V_0)^{\alpha}$.

To demonstrate the validity of using stretch-exponential model to simulate the BTS results. we further repeated the BTS tests under different $V_{G_{\rm stress}}$ (14–20 V for positive BTS, $-12 \sim -20$ V for negative BTS) and temperatures ($T_{STR} = 50$ °C ~ 80 °C for positive BTS, $= 60$ °C ~ 80 °C for negative BTS). The α is first extracted from the $\log(|\Delta V_{\rm th}|)$ versus $\log(|\Delta V_0|)$ plots as depicted in Fig. 12. The extracted α for positive BTS ($= 1.41$) is larger than the one extracted for negative BTS ($= 1.3$); this result suggests that the $\Delta V_{\rm th}$ for positive BTS is more sensitive to $V_{G_{\rm stress}}$. Figs. 13 and 14 show the evolution of $\Delta V_{\rm th}$ as a function of stress time ($t_{\rm stress}$) under different positive and negative BTS conditions, respectively. The dash lines in these two figures are the numerical fits to (16). The characteristic trapping time, τ, is treated as fitting parameter and plotted as a function of $1/kT_{STR}$ in Fig. 15. Simulation errors were observed for data points with short stress time ($< 10^3$ s); this is because the $\Delta V_{\rm th}$ for these data points are very close to the measurement resolution (~ 0.2 V) set in

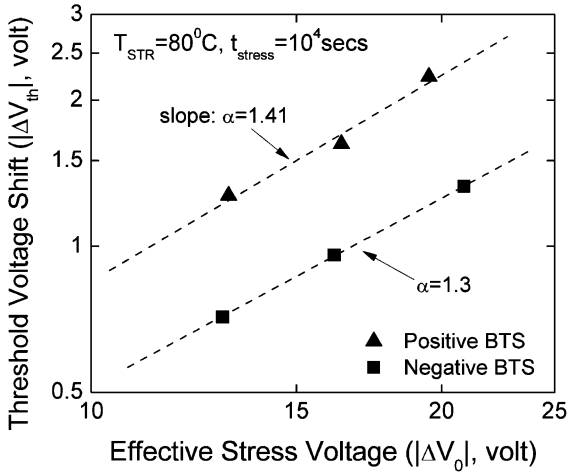

Fig. 12. $\Delta V_{\rm th}$ as a function of effective stress voltage (ΔV_0) for positive (symbol: ▲) and negative (■) BTS. Dash lines are the linear fit to the experimental data.

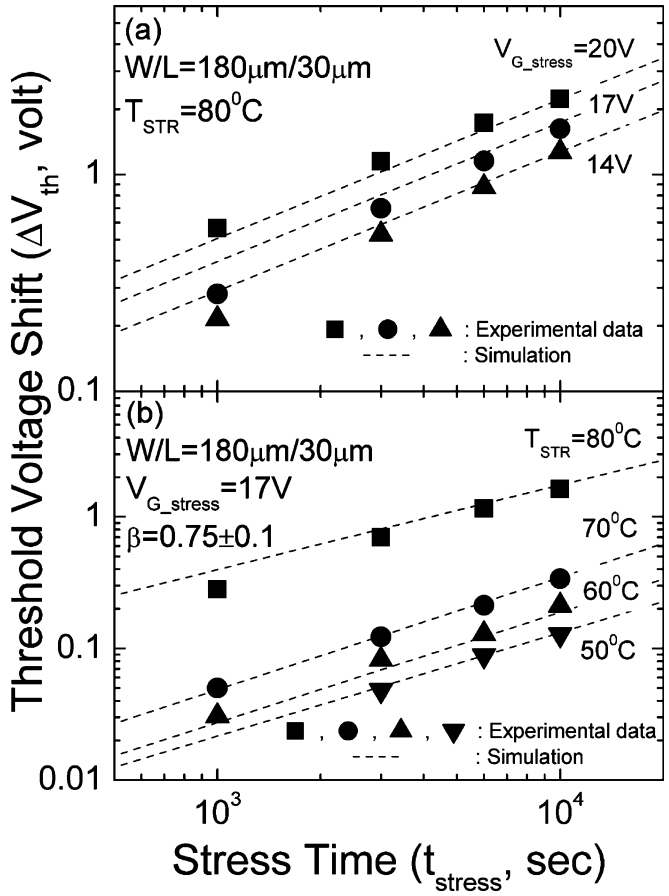

Fig. 13. $\Delta V_{\rm th}$ vs stress time ($t_{\rm stress}$) for various (a) positive stress voltages ($V_{G\_\rm stress}$ = 20 V, 17 V and 14 V, T_{STR} = 80 °C) and (b) temperature (T_{STR} = 50 °C ∼ 80 °C, $V_{G\_\rm stress}$ = 17 V). Symbols represent the experimental data while dashed lines are the simulation fits to stretched-exponential model ((16)).

this study. Despite the errors, the stretched-exponential model is able to universally reproduce the trend of experimental data, regardless of magnitude of the stress voltage, BTS polarity or stress temperature. This implies that the carrier injection from conducting channel and the subsequent charge trapping plays

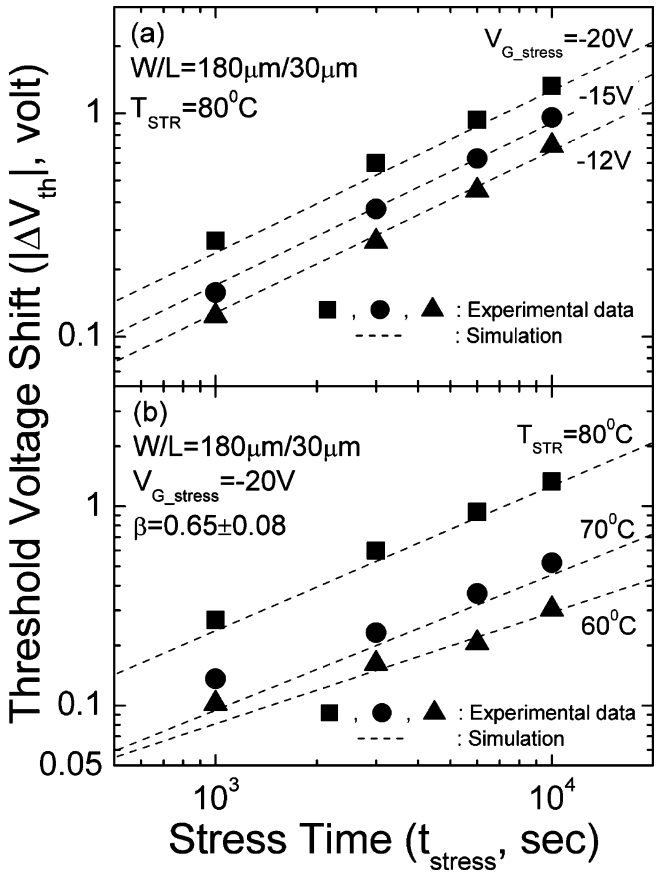

Fig. 14. $\Delta V_{\rm th}$ vs stress time ($t_{\rm stress}$) for various (a) negative stress voltages ($V_{G\_\rm stress}$ = −20 V, −15 V and −12 V, T_{STR} = 80 °C) and (b) temperature (T_{STR} = 60 °C ∼ 80 °C, $V_{G\_\rm stress}$ = −20 V). Symbols represent the experimental data while dashed lines are the simulation fits to stretched-exponential model ((16)).

an important role in the a-IGZO TFT BTS instability. Such conclusion is also consistent with the discussion in previous section.

To determine the exact $\Delta V_{\rm th}$ dependence on stress temperature, we extract the E_τ and τ_0 by applying (18) to the τ versus $1/kT_{STR}$ plots (Fig. 15). Table II summarizes all the parameters used in the stretched-exponential model. The extracted E_τ for positive BTS (0.78 eV) is smaller than the value of negative BTS (2.16 eV). This suggests that the electrons are experienced a lower energy barrier than holes do during the charge injection process near the a-IGZO/SiO_2 interface. Electron injection is very efficient and can quickly fill out the available states which in-turn increases the chance for re-emitting these filled states. As a result, the characteristic trapping time (τ) for positive BTS $\Delta V_{\rm th}$ to reach the saturation point is lower than the values of negative BTS. It should be noticed that there is an exponential dependence of τ_0 on the y-axis intercept of the linear fit of data in Fig. 15. Therefore, the extracted τ_0 can be very sensitive to the y-axis intercept and error can occur in our extraction due to the limited number of data points. More temperature dependence BTS data will be necessary to accurately determine the τ_0.

Although the stretched-exponential model predicted $\Delta V_{\rm th} \rightarrow (\Delta V_0)^\alpha$ for long stress time, we didn't observed a strong saturated behavior with $\Delta V_{\rm th}$, since the BTS only performed for

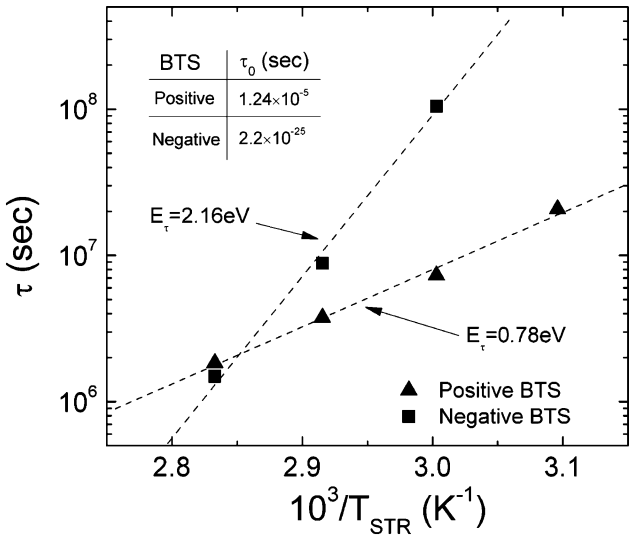

Fig. 15. Characteristic trapping time τ for positive (symbol: ▲) and negative (■) BTS as a function of $1/T_{STR}$. ($T_{\rm STR}$ range: 50 °C–80 °C). Dash line: numerical fit to (18).

$t_{\rm stress}$ upto 10 Ks in our experiments (e.g., limited stress time). The β listed in Table II is close ($< 8\%$ difference) to the average value extracted from the $\log(\Delta V_{\rm th})$ vs $\log(t_{\rm stress})$ plot based on (19) (for example, in positive BTS, $\beta \sim 0.76$; in negative BTS, $\beta \sim 0.7$). This also suggests that the short stressing time assumption ($t_{\rm stress} \ll \tau$) is generally valid in this study. A small variation (0.1 & 0.08 for positive and negative BTS, respectively) is observed for β extracted from positive and negative BTS data under different $T_{\rm STR}$ with the average β of 0.75 and 0.65, respectively. In summary, our proposed analytical equation can not only serve as a universal model for describing the RF sputter a-IGZO TFT BTS instability but also provide valuable insights on the actual physical mechanism governing the observed instability.

VI. Conclusion

A detail analysis on RF sputter a-IGZO TFT DC electrical properties was performed. The $\mu_{\rm eff}$ of a-IGZO TFT is observed to be gate voltage dependent and we proposed a nonlinear model for accurately modeling the TFT *I–V* properties. The nonideal value of $\gamma > 1$ is originated from the existence of conduction band-tail states and the characteristic temperature (T_G) of these states is extracted to be ~ 371 K (or $kT_G \sim 32$ meV).

To understand the device electrical instability, a systematic BTS study of RF sputter a-IGZO TFT was conducted. Both positive and negative BTS are applied and found to cause a positive and negative shift in transfer characteristics, respectively. By monitoring the time evolution of $\Delta V_{\rm th}$, γ and sub-threshold swing (S), we were able to conclude that both conduction-band tail states and deep bulk states experienced only minor changes and the carrier injection/trapping was the dominated mechanism for a-IGZO TFT BTS instability.

For the ease of future modeling of BTS instability or lifetime prediction of a-IGZO TFT, we have demonstrated that the stretched-exponential equation can be used to model the BTS induced $\Delta V_{\rm th}$. The model can also predict the dependence of $\Delta V_{\rm th}$ evolution on stress voltage $(V_{G\_\rm stress})$ and temperature (T_{STR}). In addition, through the analysis of characteristic trapping time (τ) on temperature, we found the electron encounters a lower energy barrier which implies that the electron-injection into state located near oxide/a-IGZO channel or oxide gate dielectric can be more efficient than hole-injection during the BTS experiments. The observation is similar to the case of c-Si MOSFET where barrier height for hole injection into the oxide is larger than electron injection. [41].

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